REMARKS

Claims 1-5 are pending in this application, all of which have been amended. No new claims have been added.

Claims 1-2 stand rejected under 35 U.S.C. §103(a) as anticipated by U.S. Publication 05-067810 to **Nakamura** (hereafter "**Nakamura**") in view of U.S. Patent 5,313,141 to **Kimball** (hereafter "**Kimball**").

Applicant respectfully traverses this rejection.

Nakamura discloses a drive circuit for LED by connecting two or more circuit blocks in series, each block being constituted by connecting one end of a light emitting diode with one end of a bypassing circuit and by making a connection with changeover circuit which permits a current to flow to the light emitting diode side or to the bypassing circuit side. A circuit block is constituted by a limiting resistor 1 which limits the current flowing in the entire circuit, a switch 2 which dims all light emitting diodes and switches 20, 21,...29 which select to which the current is permitted to flow, light emitting diodes 30, 31,...39 or bypassing resistors 10, 11,...19. Ten blocks are connected in series. The light emitting diode 39 is turned on by changing the switch 29 over to the light emitting diode side. And it is dimmed by changing the switch over to the resistor 19 side. This applies to other light emitting diodes, too. As a result, power consumption is reduced.

FIG. 1 of **Nakamura** shows each circuit block in series, where a single resistor is arranged in parallel with each LED and a switch 20, 21,...29 switches between one or the other. No constant circuit current is shown in FIG. 1, as recited in claim 1 of the instant application. However, FIG. 2 shows constant circuit current 3, but no resistors in parallel with the LED, as recited in claim 1 of the instant application.

Kimball discloses an inverter for powering an electroluminescent lamp having a direct current supply terminal, a ground terminal, and a single output terminal. A high frequency pumping circuit stores electrical energy in an inductor having a first terminal and a second terminal. A switching circuit alternately connects the first and

second terminals of the inductor to the output terminal at a low frequency. The output from the inverter is a high voltage, low frequency, alternating current.

Kimball was cited for teaching "that it was well known in the art to provide that the corresponding switching element and the corresponding switching element are controlled to be opened and closed in opposite ways."

Even if it is admitted that **Kimball** provides such a teaching, no single embodiment of **Nakamura** provides both the constant current circuit and at least two circuit blocks having a resistor circuit and an LED circuit in parallel, as recited in claim 1 of the instant application. It would not be obvious to add the parallel resistor in each block taught in FIG. 1 to each parallel LED/switch block of FIG. 2 because paragraph [0013] discloses that the bypass circuit is "made from resistance of the switches 40 and 0 ohm connected to juxtaposition at it."

In the arrangement recited in claim 1, a desired voltage can be applied to the respective display LEDs, and the number of constant current circuits can be reduced, and, hence, a reduction of power consumption and a resulting reduced cost is achieved.

In the arrangement recited in claim 2, flowing electric current can easily be cut off when both of the display LEDs connected serially are in OFF state, and a reduction of current consumption and a resulting reduced cost is achieved.

Thus, the 35 U.S.C. §103(a) rejection should be withdrawn.

Claim 3 stands rejected under 35 U.S.C. §103(a) as unpatentable over **Nakamura** in view of U.S. Patent Publication 2004/0046673 to **Kovarik et al.** (hereafter "**Kovarik et al.**") and further in view of **Kimball**.

Applicant respectfully traverses this rejection.

The Examiner has admitted that **Nakamura** fails to teach the constant voltage diode and an output terminal for delivering voltage between the display LED

circuit and the constant voltage diode, but has cited **Kovarik et al.** for teaching the feature.

Applicant respectfully disagrees. **Kovarik et al.** discloses a voltage indicator circuit for indicating a charge state of a power supply, such as a battery pack. The voltage indicator circuit includes a voltage divider circuit that connects to a plurality of series connected light sources, such as light emitting diodes. Upon activation of the voltage divider circuit, one or more of the light sources may illuminate to provide a visual indication of the current charge state of the power supply.

As noted above for claim 1, no single embodiment of **Nakamura** shows both the constant current circuit and the serially connected circuit block formed of a parallel arrangement of a resistor circuit and an LED circuit, as recited in claim 3.

In the arrangement recited in claim 3, improvement of the power source usage efficiency is achieved.

Thus, the 35 U.S.C. §103(a) rejection should be withdrawn.

Claim 4 stands rejected under 35 U.S.C. §103(a) as unpatentable over U.S. patent 4,355,308 to **Blossfeldt** (hereafter "**Blossfeldt**"), in view of U.S. patent 4,198,629 to **Marion** (hereafter "**Marion**"), and further in view of **Nakamura**, **Kovarik et al.**, and **Kimball**.

Applicant respectfully traverses this rejection.

Blossfeldt discloses a circuit for operating opto-electrical display elements assigned to terminal devices for displaying switching states and/or operating states, control switch-luminescent diode combinations are connected at intersections of row drive lines and column drive lines so that application of appropriate potentials to the drive line cause selective energization of the luminescent diodes. A plurality of controllable semiconductor switches are connected to be driven by the column drive lines and are connected to shunt those control switch-luminescent diode combinations which are not to be activated. A current limiting circuit is connected between the

luminescent diodes and a supply voltage and is operable from a low ohmic state to a high ohmic state in response to switch-through of all of the controllable semiconductor switches.

Marion discloses a numerical display having a reduced dc current requirement per character display site. The applicable displays include seven segment and 4x7 matrix displays using light emitting diodes, and low voltage incandescent segmented units designed to replace light emitting diode displays. A practical application is for displaying time in an ac powered clock or clock radio in which it is desirable to deep the dc current requirement of the display to a substantially constant minimum suitable for use with a low cost, transformerless power supply conventional with radio receivers. The current requirement of a character display site is reduced over that of full parallel operation by selectively serializing certain light sources in a manner leaving the display control circuitry uncomplicated by permitting each light source state to be controlled by a shunt control switch sharing a common bus. Since a seven segment display may assume 2^7 or 128 characters and only 10 (or 11) characters are used in a full numerical font, considerable control flexibility may be sacrificed by serial segment connection before any useful characters are eliminated. A display site having a full numerical font may be reduced 43% relative to full parallel operation under shunt control. Shunt control, which diverts, rather than prevents, current flow in the display, permits the display current to remain substantially constant irrespective of the numbers displayed. When the dc current drain of a time display is comparable to that of a radio and the ac component is tolerably low, the two may be serially connected without substantially increasing the dissipation over that of the clock or the radio alone.

It should be initially noted that claim 4 is a more detailed and narrower version of claim 1, where both claims cover the embodiment shown in FIG. 1 of the instant application.

Although **Blossfeldt** discloses serially connected circuit blocks, each containing an LED, the resistors (R1-R4) shown in the FIGURE are connected to the bases of transistor switches T1-T4, respectively, and are therefore not connected in

parallel with LEDs 1-4, each of which is connected to the collector of one of transistors T1-T4. This is in contrast to claim 4 of the present invention, which recites this parallel arrangement of the resistor circuit and LED circuit in each serially connected circuit block.

Although **Marion** was cited to teach a second constant current circuit, **Marion** also fails to disclose this specific circuit arrangement described above.

As noted above, FIG. 2 of **Nakamura** fails to teach the use of a parallel resistor/LED arrangement for each circuit block when a constant current circuit is used. **Kovarik et al.** and **Kimball** also fail to teach, mention or suggest this particular circuit arrangement.

In the arrangement recited in claim 4, improvement in the power source usage efficiency is achieved, resulting in reduced power consumption and lower costs.

Thus, the 35 U.S.C. §103(a) rejection should be withdrawn.

Claim 5 stands rejected under 35 U.S.C. §103(a) as unpatentable over **Blossfeldt** in view of **Marion**, **Nakamura**, **Kovarik et al.** and **Kimball**, and further in view of U.S. Patent 6,320,322 to **Tanaka** (hereafter "**Tanaka**").

Applicant respectfully traverses this rejection.

Tanaka discloses a light emitting appliance having a blue light emitting element B and green light emitting element G coupled in series with each other to constitute a ring. The coupling points of these elements are used as a first connecting point 24 and a second connecting point 26. The one electrode of a red light emitting element R is connected to the first input terminal 24 and the other electrode thereof is used as a third terminal. By adjusting the voltages to be applied to the input terminals 24, 26 and 28, the light emitting state of each light emitting element is adjusted.

Tanaka has been cited for teaching that one of the first and the third display LEDs is a green display LED (G), and the other one is a blue display LED (column 8,

lines 26-42; figure 4A) but, like the other cited references, fails to teach, mention or suggest the limitations recited in claim 4, from which claim 5 depends.

In the arrangement recited in claim 5, voltage drop may be averaged, and the required power source voltage may be lowered to reduce the load to the drive circuit.

Thus, the 35 U.S.C. §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-5, as amended, are in condition for allowance, which action, at an early date, is respectfully solicited.

The Director is hereby authorized to charge any deficiency in the fees filed, asserted to be filed or which should have been filed herewith (or with any paper hereafter filed in this application by this firm) to our Deposit Account No. 04-1105.

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Respectfully submitted,

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